Claims

[c1] 1. An electronic device, comprising:
a source and a drain;
a single-crystal first fin having first and second opposing ends and first and second opposing sidewalls and extending along a first longitudinal axis from said first to said second end of said first fin, said first end of said first fin in contact with said source and said second end of said first fin in contact with said drain, said first longitudinal axis aligned to a crystal plane;
a single-crystal second fin having first and second opposing ends and first and second opposing sidewalls and extending along a second longitudinal axis from said first to said second end of said second fin, said first end of said second fin in contact with said source and said second end of said second fin in contact with said drain, said second longitudinal axis aligned in a plane rotated away from said crystal plane; and
a conductive gate in contact with a gate dielectric formed on said first and second sidewalls of said first fin and on said first and second sidewalls of said second fin.

[c2] 2. The device of claim 1, wherein said crystal plane has

orthogonal first and second axes, said plane has orthogonal first and second axes and said first axis of said crystal plane and said first axis of said plane are mutually parallel.

[c3] 3. The device of claim 1, wherein said source and said drain are doped N-type, said first fin and said second fin independently comprise P-doped, lightly N-doped or intrinsic mono-crystalline silicon, said crystal plane is a {100} crystal-plane and said plane is rotated toward a {110} crystal plane.

[c4] 4. The device of claim 1, wherein said source and said drain are doped P-type, said first fin and said second fin independently comprise N-doped, lightly P-doped or intrinsic mono-crystalline silicon, said crystal plane is a {110} crystal-plane and said plane is rotated toward a {100} crystal plane.

[c5] 5. The device of claim 1, wherein said device has a drive strength, said drive strength being a function of an angle between said first longitudinal axis and said second longitudinal axis.

[c6] 6. The device of claim 1, wherein a mobility of inversion carriers along said first longitudinal axis is greater than a mobility of inversion carriers along said second longitu-

dinal axis.

[c7] 7. A method for tuning the drive strength of an electronic device, comprising:
forming a source and a drain in a single-crystal material;
forming a single-crystal first fin from said single-crystal material, said first fin having first and second opposing ends and first and second opposing sidewalls and extending along a first longitudinal axis from said first to said second end of said first fin, said first end of said first fin in contact with said source and said second end of said first fin in contact with said drain;
aligning said first longitudinal axis to a crystal-plane of said single-crystal material;
forming a single-crystal second fin from said single-crystal material, said second fin having first and second opposing ends and first and second opposing sidewalls and extending along a second longitudinal axis from said first to said second end of said second fin, said first end of said second fin in contact with said source and said second end of said second fin in contact with said drain;
aligning said second longitudinal axis to a plane rotated away from said crystal plane; and

providing a conductive gate in contact with a gate dielectric formed on said first and second sidewalls of said first fin and on said first and second sidewalls of said second fin.

[c8] 8. The method of claim 7, wherein said crystal plane has orthogonal first and second axes, said plane has orthogonal first and second axes and said first axis of said crystal plane and said first axis of said plane are mutually parallel.

[c9] 9. The method of claim 7, wherein said source and said drain are doped N-type, said first fin and said second fin independently comprise P-doped, lightly N-doped or intrinsic, said crystal plane is a {100} crystal-plane and said plane is rotated toward a {110} crystal-plane.

[c10] 10. The method of claim 7, wherein said source and said drain are doped P-type, said first fin and said second fin independently comprise N-doped, lightly P-doped or intrinsic mono-crystalline silicon, said crystal-plane is a {110} crystal-plane and said plane is rotated toward a {100} crystal-plane.

[c11] 11. The method of claim 7, wherein said device has a drive strength, said drive strength being a function of an angle between said first longitudinal axis and said sec-

ond longitudinal axis.

[c12] 12. The method of claim 7, wherein a mobility of inversion carriers along said first longitudinal axis is greater than a mobility of inversion carriers along said second longitudinal axis.

[c13] 13. An integrated circuit, comprising:

a first transistor comprising:

a first source and a first drain;

a single-crystal first fin having first and second opposing ends and first and second opposing sidewalls and extending along a first longitudinal axis from said first to said second end of said first fin, said first end of said first fin in contact with said first source and said second end of said first fin in contact with said first drain, said first longitudinal axis aligned to a crystal plane;

a single-crystal second fin having first and second opposing ends and first and second opposing sidewalls and extending along a second longitudinal axis from said first to said second end of said second fin, said first end of said second fin in contact with said first source and said second end of said second fin in contact with said first drain, said second longitudinal axis aligned in a plane rotated away from said crystal plane; and

a first conductive gate in contact with a gate dielectric formed on said first and second sidewalls of said first fin and on said first and second sidewalls of said second fin; and

a second transistor comprising:

a second source and a second drain;

a single-crystal third fin having first and second opposing ends and first and second opposing sidewalls and extending along a third longitudinal axis from said first to said second end of said third fin, said first end of said third fin in contact with said second source and said second end of said first fin in contact with said second drain, said third longitudinal axis aligned to said crystal plane; and

a second conductive gate in contact with a gate dielectric formed on said first and second sidewalls of said third fin and on said first and second sidewalls of said third fin.

[c14] 14. The circuit of claim 13, wherein said crystal plane has orthogonal first and second axes, said plane has orthogonal first and second axes and said first axis of said crystal plane and said first axis of said plane are mutually parallel.

[c15] 15. The circuit of claim 13, wherein said first source and said first drain are doped N-type, said second source

and said second drain are doped P-type, said first fin and said second fin independently comprise P-doped, lightly N-doped or intrinsic mono-crystalline silicon, said third fin comprises N-doped, lightly P-doped or intrinsic mono-crystalline silicon, said crystal plane is a {100} crystal-plane and said plane is rotated toward a {110} crystal plane.

[c16] 16. The circuit of claim 13, wherein said first source and said first drain are doped P-type, said second drain and said second source are doped N-type, said first fin and said second fin independently comprise N-doped, lightly P-doped or intrinsic mono-crystalline silicon, said third fin comprises P-doped, lightly N-doped or intrinsic mono-crystalline silicon, said crystal plane is a {110} crystal-plane and said plane is rotated toward a {100} crystal plane.

[c17] 17. The circuit of claim 13, wherein a drive strength ratio between said first transistor and said second transistor is a function of an angle between said first longitudinal axis and said second longitudinal axis.

[c18] 18. The circuit of claim 13, wherein a mobility of inversion carriers along said first longitudinal axis is greater than a mobility of inversion carriers along said second longitudinal axis.

[c19] 19. A method of tuning the drive strength ratio between a first transistor and a second transistor in an integrated circuit, comprising:

providing said first transistor, said first transistor comprising:

a first source and a first drain;

a single-crystal first fin having first and second opposing ends and first and second opposing sidewalls and extending along a first longitudinal axis from said first to said second end of said first fin, said first end of said first fin in contact with said first source and said second end of said first fin in contact with said first drain, said first longitudinal axis aligned to a crystal plane;

a single-crystal second fin having first and second opposing ends and first and second opposing sidewalls and extending along a second longitudinal axis from said first to said second end of said second fin, said first end of said second fin in contact with said first source and said second end of said second fin in contact with said first drain, said second longitudinal axis aligned in a plane rotated away from said crystal plane; and

a first conductive gate in contact with a gate dielectric formed on said first and second sidewalls of said

first fin and on said first and second sidewalls of said second fin; and

providing said second transistor, said second transistor comprising:

a second source and a second drain;

a single-crystal third fin having first and second opposing ends and first and second opposing sidewalls and extending along a third longitudinal axis from said first to said second end of said third fin, said first end of said third fin in contact with said second source and said second end of said first fin in contact with said second drain, said third longitudinal axis aligned to said crystal plane; and

a second conductive gate in contact with a gate dielectric formed on said first and second sidewalls of said third fin and on said first and second sidewalls of said third fin.

[c20] 20. The method of claim 19, wherein said crystal plane has orthogonal first and second axes, said plane has orthogonal first and second axes and said first axis of said crystal plane and said first axis of said plane are mutually parallel.

[c21] 21. The method of claim 19, wherein said first source and said first drain are doped N-type, said second source and said second drain are doped P-type, said first

fin and said second fin independently comprise P-doped, lightly N-doped or intrinsic mono-crystalline silicon, said third fin comprises N-doped, lightly P-doped or intrinsic mono-crystalline silicon, said crystal plane is a {100} crystal-plane and said plane is rotated toward a {110} crystal plane.

[c22] 22. The method of claim 19, wherein said first source and said first drain are doped P-type, said second drain and said second source are doped N-type, said first fin and said second fin independently comprise N-doped, lightly P-doped or intrinsic mono-crystalline silicon, said third fin comprises independently comprise P-doped, lightly N-doped or intrinsic mono-crystalline silicon, said crystal plane is a {110} crystal-plane and said plane is rotated toward a {100} crystal plane.

[c23] 23. The method of claim 19, wherein said drive strength ratio between said first transistor and said second transistor is a function of an angle between said first longitudinal axis and said second longitudinal axis.

[c24] 24. The method of claim 19, wherein a mobility of inversion carriers along said first longitudinal axis is greater than a mobility of inversion carriers along said second longitudinal axis.

[c25] 25. An electronic device, comprising:

a source and a drain;

a single-crystal first fin having first and second opposing ends and first and second opposing sidewalls, said first end of said first fin in contact with said source and said second end of said first fin in contact with said drain, said first longitudinal axis aligned to a crystal plane;

a single-crystal second fin having first and second opposing ends and first and second opposing sidewalls, said first end of said second fin in contact with said source and said second end of said second fin in contact with said drain;

a first conductive gate in contact with a gate dielectric formed on said first and second sidewalls of said first fin and on said first sidewall of said second fin; and

a second conductive gate in contact with a gate dielectric formed on said second sidewall of said second fin.

[c26] 26. The device of claim 25, wherein said source and said drain are doped N-type, said first fin and said second fin independently comprise intrinsic, lightly N-doped or P-doped mono-crystalline silicon.

[c27] 27. The device of claim 26, wherein first and second fins are aligned in a direction from respective said first ends of said first and said second fins to respective said second ends of said first and said second fins to a {100} crystal-plane.

[c28] 28. The device of claim 26, wherein said source and said drain are doped P-type, said first fin and said second fin independently comprise intrinsic, N-doped or lightly P-doped mono-crystalline silicon.

[c29] 29. The device of claim 28, wherein first and second fins are aligned in a direction from respective said first ends of said first and second fin to respective said second ends of said first and said second fins to a {110} crystal-plane.

[c30] 30. A method for tuning the drive strength of an electronic device, comprising:

providing a source and a drain;

providing a single-crystal first fin having first and second opposing ends and first and second opposing sidewalls, said first end of said first fin in contact with said source and said second end of said first fin in contact with said drain;

providing a single-crystal second fin having first and second opposing ends and first and second opposing

sidewalls, said first end of said second fin in contact with said source and said second end of said second fin in contact with said drain;

providing a first conductive gate in contact with a gate dielectric formed on said first and second side-walls of said first fin and on said first sidewall of said second fin;

providing a second conductive gate in contact with a gate dielectric formed on said second sidewall of said second fin; and

connecting said first gate to a first voltage source at a first voltage level and connecting said second gate a second voltage source at a second voltage level, said first and second voltage levels being different.

[c31] 31. The method of claim 30, wherein said first and second voltage levels have different magnitudes, different polarities or both different magnitudes and polarities.

[c32] 32. The method of claim 30, where said drive strength is a function of a magnitude and polarity of said second voltage source.

[c33] 33. The method of claim 30, wherein said source and said drain are doped N-type, said first fin and said second fin comprise intrinsic, lightly N-doped or P-doped mono-crystalline silicon and wherein said first and said

second fins are aligned in a direction from respective said first ends of said first and said second fins to respective said second ends of said first and said second fins to a {100} crystal-plane.

[c34] 34. The method of claim 30, wherein said source and said drain are doped P-type, said first fin and said second fin independently comprise intrinsic, N-doped or lightly P-doped mono-crystalline silicon and wherein said first and said second fins are aligned in a direction from respective said first ends of said first and said second fins respective said second ends of said first and said second fins to a {110} crystal-plane.

[c35] 35. An integrated circuit, comprising:

a first transistor comprising:

a first source and a first drain;

a single-crystal first fin having first and second opposing ends and first and second opposing sidewalls, said first end of said first fin in contact with said first source and said second end of said first fin in contact with said first drain;

a single-crystal second fin having first and second opposing ends and first and second opposing sidewalls, said first end of said second fin in contact with said first source and said second end of said second fin in contact with said first drain;

a first conductive gate in contact with a gate dielectric formed on said first and second sidewalls of said first fin and on said first sidewall of said second fin; and

a second conductive gate in contact with a gate dielectric formed on said second sidewall of said second fin; and

a second transistor comprising:

a second source and a second drain;

a single-crystal third fin having first and second opposing ends and first and second opposing sidewalls, said first end of said third fin in contact with said second source and said second end of said third fin in contact with said second drain; and

a third conductive gate in contact with a gate dielectric formed on said first and second sidewalls of said third fin and on said first and second sidewall of said third fin.

[c36] 36. The circuit of claim 35, wherein said first source and said first drain are doped N-type said second source and said second drain are doped P-type, said first fin and said second fin independently comprise intrinsic, lightly N-doped or P-doped mono-crystalline silicon and said third fin comprises intrinsic, N-doped or lightly P-doped mono-crystalline silicon.

[c37] 37. The circuit of claim 36, wherein first and second fins are aligned in a direction from respective said first ends of said first and said second fins to respective said second ends of said first and said second fins to a {100} crystal-plane and said third fin is aligned in a direction from said first end to said second end of said third fin to a {110} crystal-plane.

[c38] 38. The circuit of claim 35, wherein said first source and said first drain are doped P-type, said second source and said second drain are doped N-type, said first fins and said second fin independently comprise intrinsic, N-doped or lightly P-doped mono-crystalline silicon and said third fin comprises intrinsic, lightly N-doped or P-doped mono-crystalline silicon.

[c39] 39. The circuit of claim 38, wherein first and second fins are aligned in a direction from respective said first ends of said first and said second fins to respective said second ends of said first and said second fins to a {110} crystal-plane and said third fin is aligned in a direction from said first end to said second end of said third fin to a {100} crystal-plane.

[c40] 40. A method of tuning the drive strength ratio between a first transistor and a second transistor in an

integrated circuit, comprising:

providing said transistor, said first transistor comprising:

a first source and a first drain;

a single-crystal first fin having first and second opposing ends and first and second opposing sidewalls, said first end of said first fin in contact with said first source and said second end of said first fin in contact with said first drain;

a single-crystal second fin having first and second opposing ends and first and second opposing sidewalls, said first end of said second fin in contact with said first source and said second end of said second fin in contact with said first drain;

a first conductive gate in contact with a gate dielectric formed on said first and second sidewalls of said first fin and on said first sidewall of said second fin; and

a second conductive gate in contact with a gate dielectric formed on said second sidewall of said second fin;

providing said second transistor, said second transistor comprising:

a second source and a second drain;

a single-crystal third fin having first and second opposing ends and first and second opposing sidewalls,

said first end of said third fin in contact with said second source and said second end of said third fin in contact with said second drain; and

a third conductive gate in contact with a gate dielectric formed on said first and second sidewalls of said third fin and on said first and second sidewall of said third fin; and

connecting said first gate to a first voltage source at a first voltage level and connecting said second gate to a second voltage source at a second voltage level, said first and second voltage levels being different.

[c41] 41. The method of claim 40, wherein said first and second voltage levels have different magnitudes, different polarities or both different magnitudes and polarities.

[c42] 42. The method of claim 40, where said drive strength is a function of a magnitude and polarity of said second voltage source.

[c43] 43. The method of claim 40, wherein said first source and said first drain are doped N-type said second source and said second drain are doped P-type, said first fin and said second fin independently comprise intrinsic, lightly N-doped or P-doped mono-crystalline silicon and said third fin comprises intrinsic, N-doped or lightly P-doped mono-crystalline silicon.

[c44] 44. The method of claim 43, wherein first and second fins are aligned in a direction from respective said first ends of said first and said second fins to respective said second ends of said first and said second fins to a {100} crystal-plane and said third fin is aligned in a direction from said first end to said second end of said third fin to a {110} crystal-plane.

[c45] 45. The method of claim 40, wherein said first source and said first drain are doped P-type, said second source and said second drain are doped N-type, said first fins and said second fin independently comprise intrinsic, N-doped or lightly P-doped mono-crystalline silicon and said third fin comprises intrinsic, lightly N-doped or P-doped mono-crystalline silicon.

[c46] 46. The method of claim 45, wherein first and second fins are aligned in a direction from respective said first ends of said first and said second fins to said second ends of said first and said second fins to a {110} crystal-plane and said third fin is aligned in a direction from said first end to said second end of said third fin to a {100} crystal-plane.